

FIG. 2

Scan path chaining which groups latches of similar types

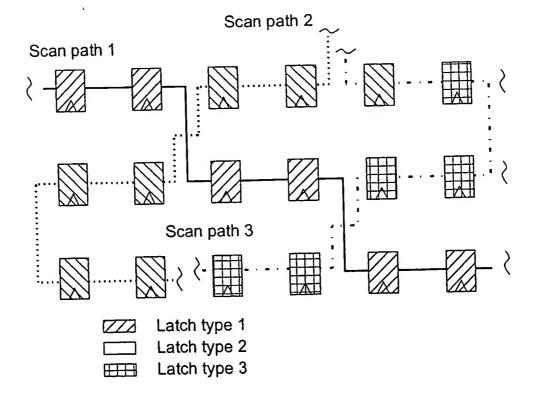


FIG. 3
Latch content optimized cell content with latch specific defect Scan path 2

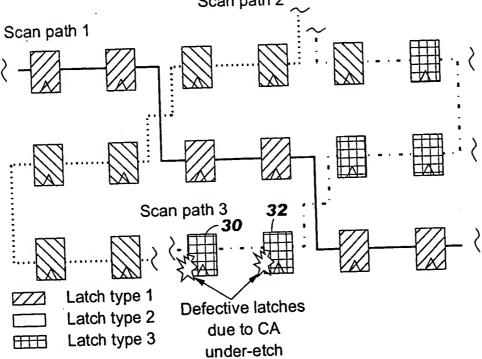
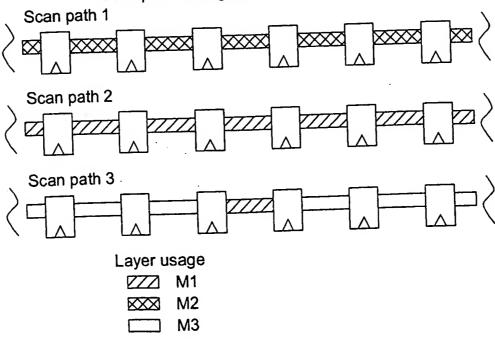
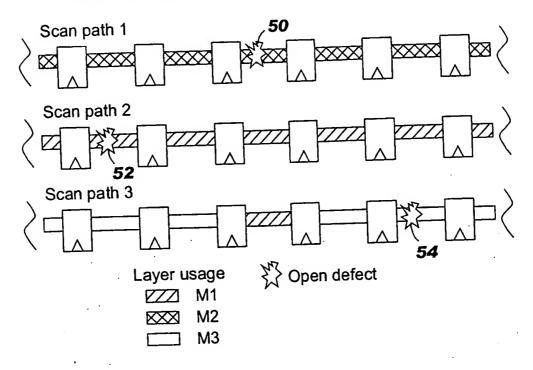


FIG. 4

Scan paths using restricted wiring layers



 $FIG.\ 5$  Layer optimized cell content with layer specific defects



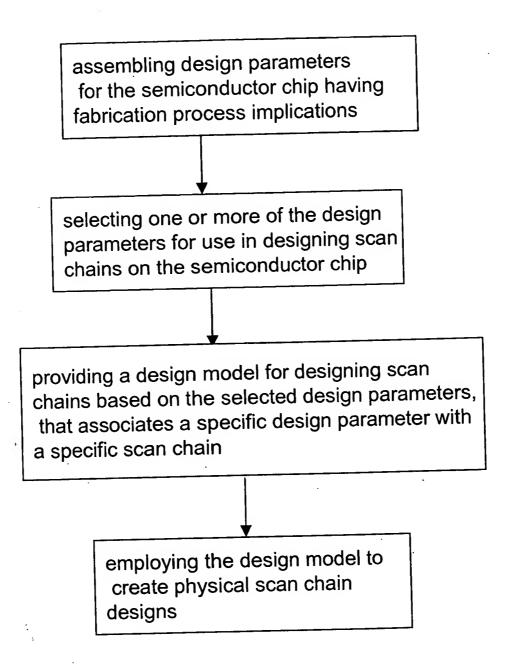


Fig. 6

analyzing specific fabrication process sensitivities of all latch cells and specific chip layer connectivity combinations in the semiconductor chip

assembling latches into scan chains while using a combination of constraints of location of latches and scan chain length, with an additional constraint of latch type to maximize latch type uniformity by scan chain

assembling latches into scan chains while biasing scan chain routing to constrain scan chain routing to given restricted interconnect layers of the semiconductor chip

analyzing scan chain failures for clustering of scan chain failures by similar content

correlating content back to a process cause based upon said scan chain failure analyzing step to create a list of likely causes of the scan chain failures

Fig. 7

assembling latch design parameters which are sensitive to process variation or integrity

formulating a design model of scan chain design based on the state of the process variation or integrity, wherein certain latch designs having dominant sensitivities are targeted to specific scan chains on the chip

providing the design model as input parameters to a global placement and wiring program used to physically implement the scan chains

analyzing global placement and wiring program test data to determine and isolate yield problems denoted by fail probabilities extracted using a statistical analysis from the passes and fails of scan chains

Fig. 8